METHOD FOR FORMING A GATE ELECTRODE ON A SEMICONDUCTOR SUBSTRATE

This application claims the benefit of Korean Application No. P2000-68405 filed Nov. 17, 2000, which is hereby incorporated by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a method for fabricating a semiconductor device, and more particularly, to a method for forming a gate electrode on a semiconductor substrate which reduces line resistance and formation of ohmic contacts.

2. Discussion of the Prior Art

Typically, to reduce gate resistance when forming a gate electrode on a semiconductor device, tungsten(W) having a specific resistance lower than WSi_x by 1 order is deposited on polysilicon. The tungsten is then patterned to form a gate electrode. However, when tungsten reacts with polysilicon at a temperature of 600° C. or greater, a silicide forms at the boundary between tungsten and polysilicon. Therefore, tungsten nitride WN_x is often used as a diffusion barrier layer between the tungsten and polysilicon, thereby forming a gate electrode having a W/WN_x/polysilicon structure.

Although WN_x is commonly used as the diffusion barrier layer, TiN may also be used. When W is deposited on TiN by a sputtering method, the grain size of W is smaller than the W/Si structure. In this scenario, resistance increases by a factor of two or more in comparison to pure W. Furthermore, the TiN is oxidized during the selective oxidation of the polysilicon layer. For these reasons, WN_x is commonly used as the diffusion barrier layer. This is disclosed by Y. Akasaka in the article, "Low-Resistivity Poly-Metal Gate Electrode Durable for High-Temperature Processing" (IEEE Trans. Electron Devices, Vol. 43, pp. 1864–1869, 1996), and by B. H. Lee in the article "In-situ Barrier Formation for High Reliable W/barrier/poly-Si Gate Using Denudation of WN_x on Polycrystalline"(IEDM, 1998).

One method for forming a gate electrode on a semiconductor device will be described with reference to the accompanying drawings.

FIGS. 1A to 1E are cross-sectional views showing the steps of a related art method for forming a gate electrode on a semiconductor device.

As shown in FIG. 1A, field oxide layers 12 are formed in a semiconductor substrate 11 in which an active region and a field region are defined. Using thermal oxidation a gate oxide layer 13 is formed on a surface of the semiconductor substrate 11 at a thickness of about 65 Å.

As shown in FIG. 1B, an undoped polysilicon layer 14 is formed by a low pressure chemical vapor deposition (LPCVD) method on the entire surface of the semiconductor substrate 11 at a thickness of about 2000 Å. N+ ions or P+ ions are then implanted into the polysilicon layer 14. When the N+ ions or P+ ions are implanted, As or P ions are implanted into a negative-channel metal oxide semiconductor (NMOS) region while B or BF_2 ions are implanted into a positive-channel metal oxide semiconductor (PMOS) region using a photoresist as a mask.

Then an annealing process is performed in the polysilicon layer 14 for ten minutes and at a temperature of 800° C. to activate the impurity ions.

As shown in FIG. 1C, the semiconductor substrate 11 is washed by HF solution and then WN_x layer 15 is formed on the polysilicon layer 14 at a thickness of 50~100 Å. A tungsten layer 16 is formed on the WN_x, layer 15 at a thickness of about 1000 Å and a first insulating layer 17 is deposited on the tungsten layer 16 at a thickness of about 2000 Å.

The WN_x layer 15 is used as a diffusion barrier between the tungsten layer 16 and the polysilicon layer 14, and the first insulating layer 17 is used as a gate cap insulating layer later.

As shown in FIG. 1D, a photoresist(not shown) is deposited on the first insulating layer 17 and then patterned by exposure and developing processes to define a gate electrode region. The first insulating layer 17, the tungsten layer 16, the WN_x layer 15, the polysilicon layer 14 and the gate oxide layer 13 are selectively removed using the patterned photoresist as a mask to form a gate electrode 18 having a structure consisting of a tungsten layer 16, a WN_x layer 15 and a polysilicon layer 14.

As shown in FIG. 1E, selective oxidation is performed in the gate electrode 18 to partially form an oxide layer (not shown) at the sides of the gate electrode 18. Then a second insulating layer is formed on the entire surface of the semiconductor substrate 11. The second insulating layer is etched back to form second insulating layer sidewalls 19 on both sides of the gate electrode 18 and the first insulating layer 17.

However, the related art method for forming a gate electrode on a semiconductor device has several problems. When W/WN_x is deposited on polysilicon, a W—Si—O—N layer forms at the boundary between tungsten and polysilicon during a later annealing process having a temperature of 800° C. or more. Thus, boundary resistance between tungsten and polysilicon increases thereby slowing the operation of the semiconductor device.

SUMMARY OF THE INVENTION

Accordingly, the present invention is directed to a method for forming a gate electrode on a semiconductor substrate that substantially obviates one or more of the problems due to limitations and disadvantages of the related art.

An object of the present invention is to provide a method for forming a gate electrode on a semiconductor substrate that reduces the boundary resistance between tungsten and polysilicon, thereby preventing the operational speed of the semiconductor device from being slowed.

Additional objects and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described, in one aspect of the present invention there is provided a method for forming a gate electrode on a semiconductor substrate that includes forming a gate insulating layer on a semiconductor substrate, forming a polysilicon layer on the semiconductor substrate, forming a tungsten silicide layer on the polysilicon layer, forming a diffusion barrier layer on the tungsten silicide layer, forming a tungsten layer on the diffusion barrier layer, crystallizing the diffusion barrier layer, forming a first insulating layer on the tungsten layer, forming a gate electrode, forming an oxide layer, and forming a second insulating layer.

formed over the interlevel dielectric layer. A bitline contact opening **186** is provided in the interlevel dielectric layer to contact the source **113** to the conductive layer **190** (bitline).

As previously discussed, the use of the poly buffer layer between the heavily doped poly and silicide layer increases the thickness of the gate stack. This increased thickness is undesirable because it produces higher aspect ratio features, creating processing difficulties.

FIGS. 2*g–c* show the process of forming a polycide gate stack in accordance with the invention. Referring to FIG. 2*a*, a schematic cross section of a substrate representing a portion of an IC is shown. Such an IC, for example, is a memory IC including a random access memory (RAM), a dynamic RAM (DRAM), a synchronous DRAM (SDRAM); a static RAM (SRAM), and a read only memory (ROMs). Also, the IC may be a logic device such as a programmable logic array (PLA), an application specific IC (ASIC), a merged DRAM-logic IC (embedded DRAM) or any other logic device.

Typically, numerous ICs are fabricated on a semiconductor substrate, such as a silicon wafer, in parallel. After processing, the wafer is diced in order to separate the ICs into a plurality of individual chips. The chips are then packaged into final products for use in, for example, consumer products such as computer systems, office equipment including copiers, printers, and facsimile systems, cellular phones, personal digital assistants (PDAs), and other electronic products.

The substrate **201** is, for example, a silicon wafer. Other substrates such as silicon on insulator (SOI), silicon on sapphire (SOS), germanium, gallium arsenide, and group III–V compounds, are also useful. In one embodiment, the substrate is lightly doped with dopants having a first conductivity. Although the substrate as shown does not include other device layers device features, it is understood that the term "substrate" as used herein may include a substrate having one or more device layers and device features thereon. In one embodiment, the substrate is lightly doped with p-type dopants (p^-), such as B. The concentration of B is about 1.5×10^{16} atoms/cm^3.

The substrate, for example, includes a plurality of trench capacitors (not shown) formed therein. The trench capacitors, for example, are those described in FIG. 1. In one embodiment, the trench capacitors serve as storage capacitors for n-channel DRAM cells. Buried n-wells are provided to connect the n-type buried plates of the capacitors together. P-wells are provided for the n-channel DRAM access transistors. The concentrations of the p-wells is about 5×10^{17}–8×10^{17} cm^{-3}. Additionally, n-type wells are provided for p-channel transistors, such as those employed in support circuitry. Other diffusion regions may be provided in the substrate as necessary.

At this point of processing, the substrate includes a planar surface **210**. A sacrificial oxide layer (not shown) is formed over the surface. The sacrificial oxide layer serves as a screen oxide for implanting ions to adjust the gate threshold voltage (V_t) of the subsequently formed transistors. The V_t adjust implant employs, for example, conventional lithographic and masking techniques to selectively implant the dopants into the channel region of the gate. Such techniques include depositing a photoresist layer over the screen oxide layer and selectively exposing it with an exposure source and mask. Depending on whether a positive or negative resist is used, either the exposed or unexposed portions of the resist layer are removed during development to selectively expose regions of the substrate below. The exposed regions are then implanted with ions to achieve the desired V_t.

After the V_t implant, the resist and screen oxide layers are removed by, for example, a wet etch. A thin oxide layer **220** is then formed on the substrate surface. The oxide layer serves as the gate oxide. In one embodiment, the gate oxide is grown by thermal oxidation. The thickness of the gate oxide is, for example, about 6–10 nm.

A poly layer **230** is deposited over the gate oxide. The poly layer is deposited by, for example, chemical vapor deposition (CVD). Alternatively, an amorpohous silicon layer can be used instead of poly. Typically, the poly layers comprise dopants to reduce its resistivity. Such dopants, for example, include phosphorus (P), arsenic (As), or boron (B). The poly layer can be doped during or after its formation. Incorporating the dopants during the CVD process is known as insitu doping.

In one embodiment, the poly layer is doped with P dopants. The poly is insitu doped. The concentration of P dopants is about 10^{19}–5×10^{21} atoms/cm^3, preferably about 10^{20}–10^{21} atoms/cm^3, and more preferably about 5×10^{20}. The poly is deposited in a CVD reactor, for example, at a temperature of about 600–650° C. and a pressure of about 100–180 Torr using SiH_4 as a silicon precursor and PH_3 as a P dopant source. The thickness of the doped poly is about 10–200 nm, preferably about 40–150 nm and, more preferably about 50–100 nm. Of course, the actual thickness can vary depending on various factors. For example, a minimum thickness is required for work function purposes and this depends on design requirements. This minimum thickness, in some cases, can be as low as about 10 nm.

Referring to FIG. 2*b*, which is a schematic cross section, a metal silicide layer **240** is deposited over the poly layer **230**. The metal silicide comprises, for example, tungsten silicide (WSi_x), molybdenum silicide ($MoSi_x$), tantalum silicide ($TaSi_x$), titanium silicide ($TiSi_x$), cobalt silicide ($CoSi_x$)., or other metal silicides. In accordance with one embodiment, the metal silicide comprises dopants, which are either p- or n-type. Such dopants include, for example, P, As, or B. The dopant type is the same, when applicable, as the doped poly layer **230**. Typical concentration of the metal silicide layer is about 10^{19}–5×10^{21} atoms/cm^3, preferably about 10^{20}–10^{21} atoms/cm^3, and more preferably 5×10^{20} atoms/cm^3. Insitu doping the metal silicide potentially increases the tendency that it will be deposited in its amorphous state. Depositing the metal silicide in its amorphous state increases the grain size of the film, thereby lowering its resistance.

The insitu doped metal silicide is deposited by conventional CVD techniques used to deposit an undoped metal silicide film. A dopant source is included in the CVD process to provide insitu doping of the deposited film.

In one embodiment, the doped metal silicide layer comprises P doped WSi_x. The WSi_x is insitu doped. The concentration of P dopants is about 10^{19}–5×10^{21} atoms/cm^3, preferably about 10^{20}–10^{21} atoms/cm^3, more preferably about 5×10^{20} atoms/cm^3. The thickness of the doped metal silicide is about 50–200 nm, preferably about 80 nm. Of course, the actual thickness can vary depending on design and parameters.

Conventional W, Si, and dopant precursors are employed to form the doped WSi_x film. Conventional Si precursors include, for example, silane (SiH_4), disilane (Si_2H_6), or dichlorosilane (SiH_2Cl_2); W precursors include tungsten hexaflouride (WF_6), tungsten hexachloride (WCl_6), or tungsten hexacarbonyl ($W[CO]_6$). Phosphine (PH_3 or $POCl_4$) is used, for example, to provide the P dopant source. In one embodiment, the PH_3 are added to WF_6 and SiH_4 to form the